

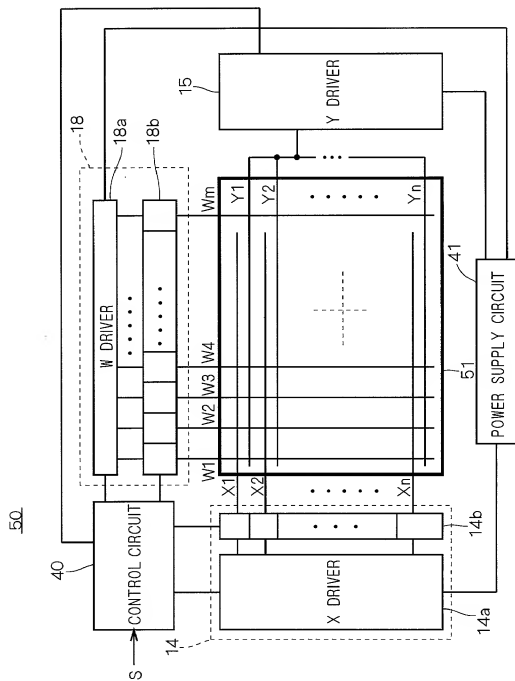
$F/G. 1$ 

FIG. 2

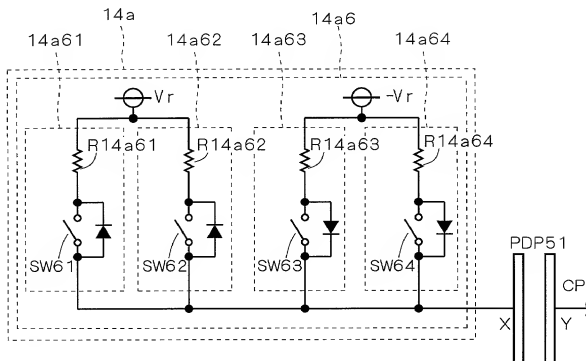


FIG. 3

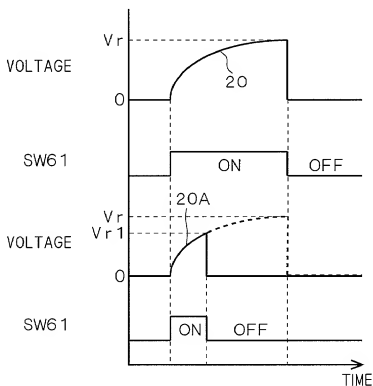


FIG. 4

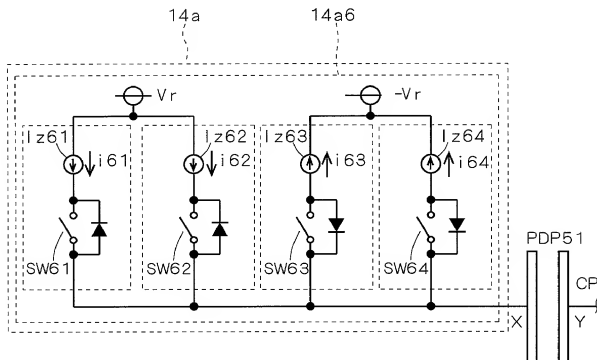


FIG. 5

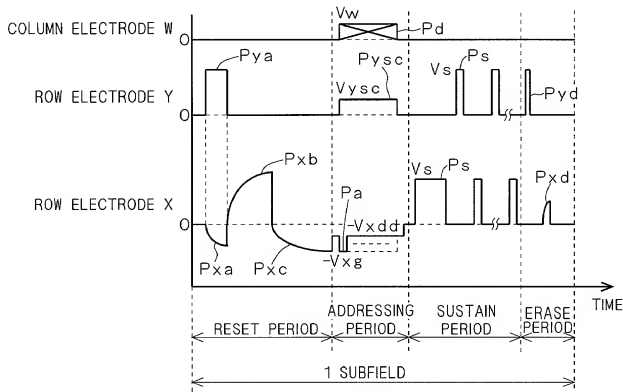


FIG. 6

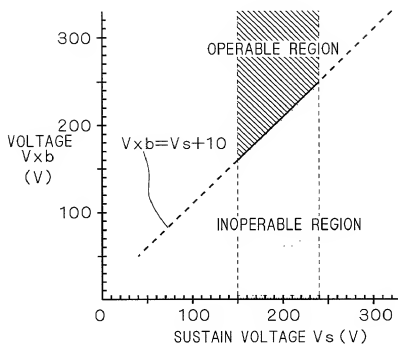


FIG. 7

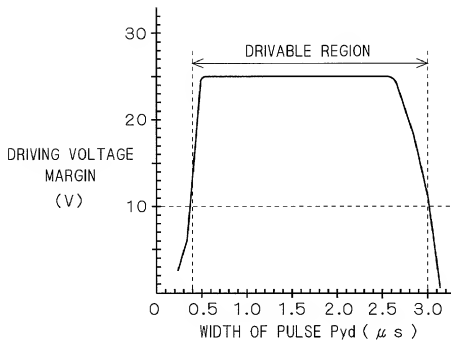


FIG. 8

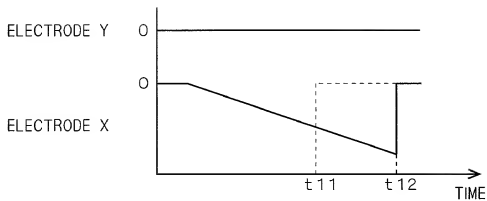


FIG. 9

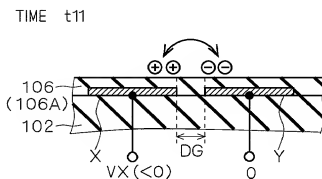


FIG. 10

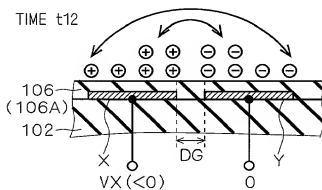


FIG. 11

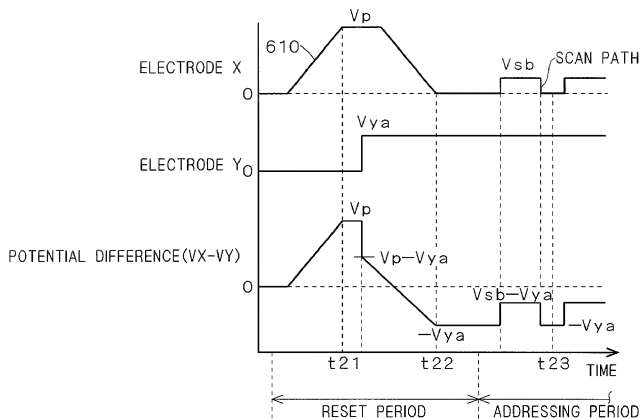


FIG. 12

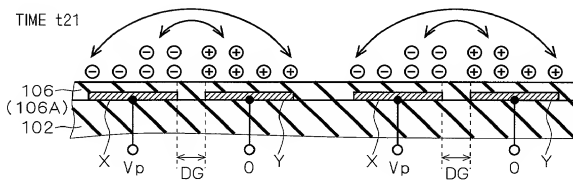


FIG. 13

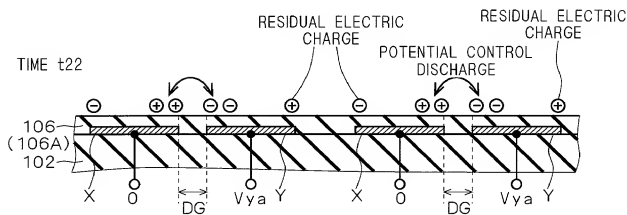


FIG. 14

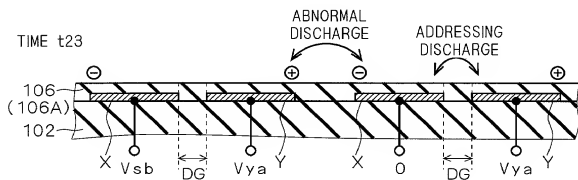


FIG. 15

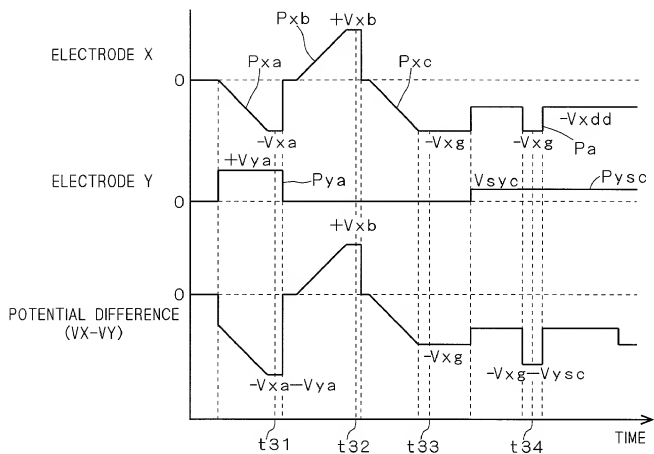


FIG. 16

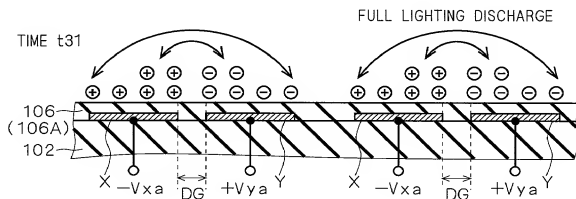




FIG. 17

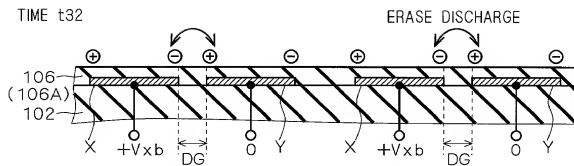


FIG. 18

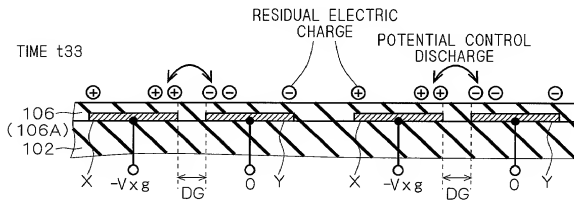


FIG. 19

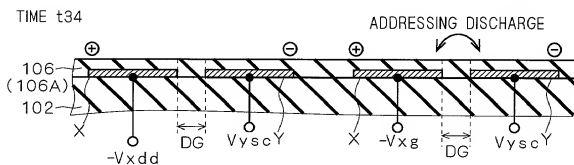


FIG. 20

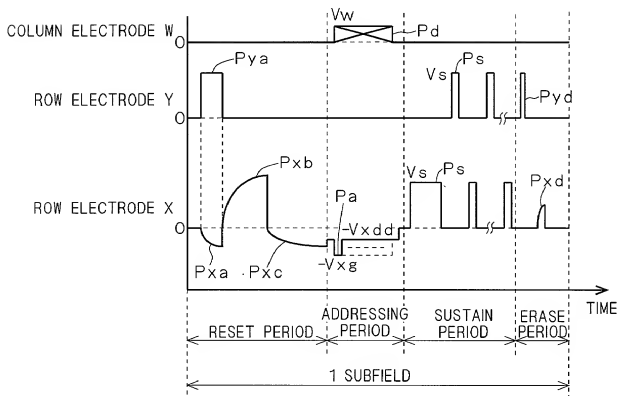


FIG. 21

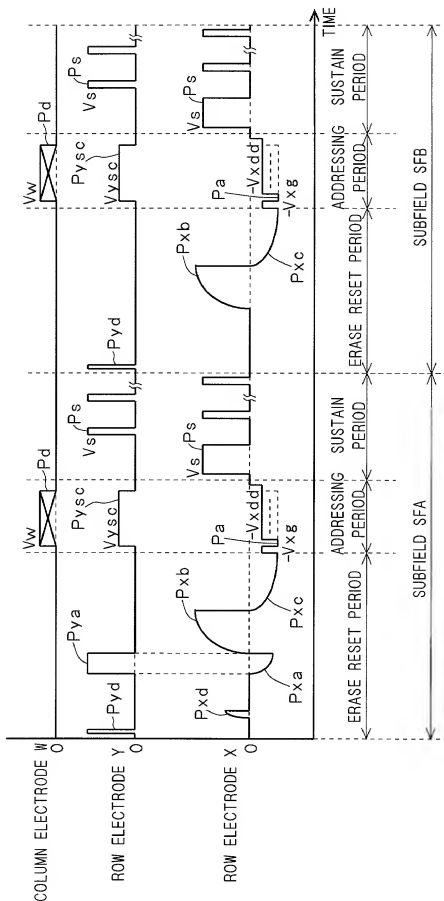


FIG. 22

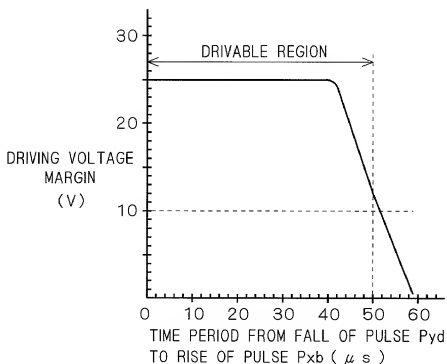


FIG. 23

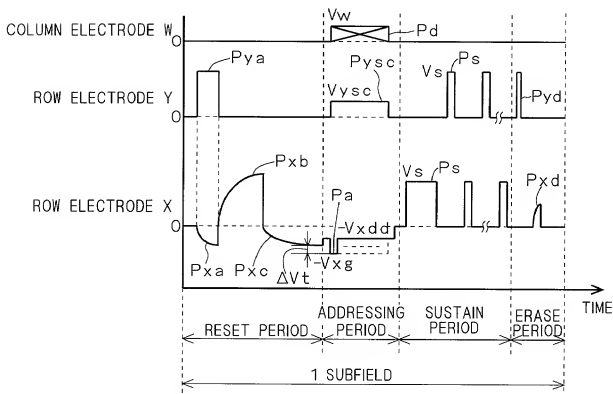


FIG. 24

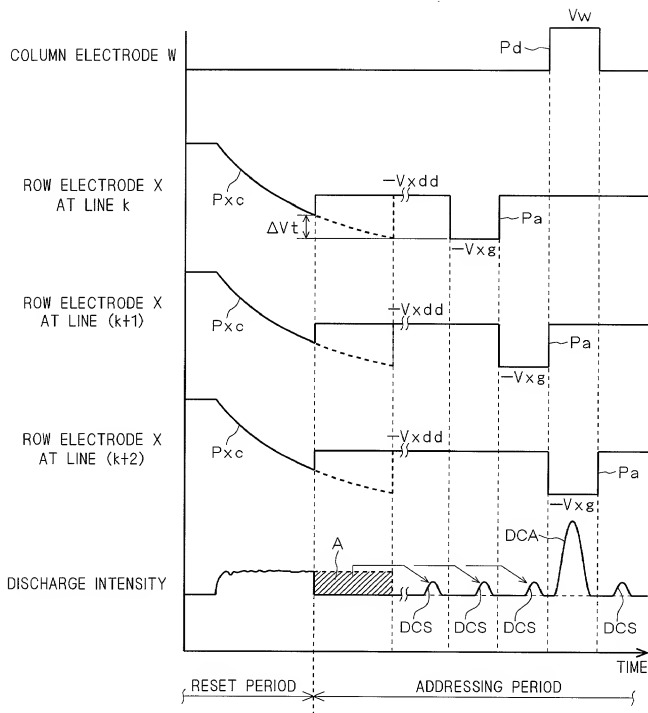


FIG. 25

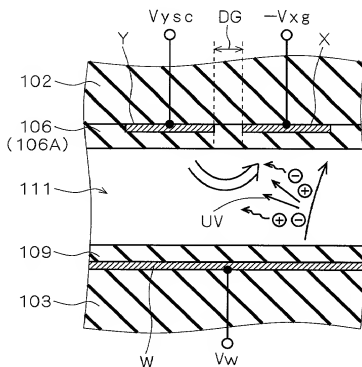


FIG. 26

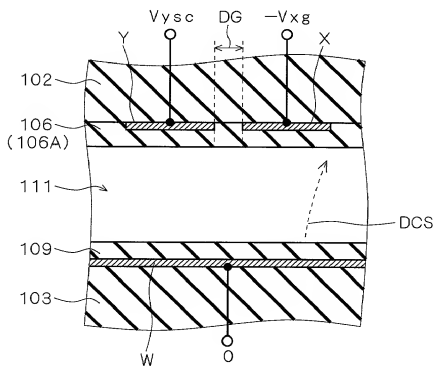


FIG. 27

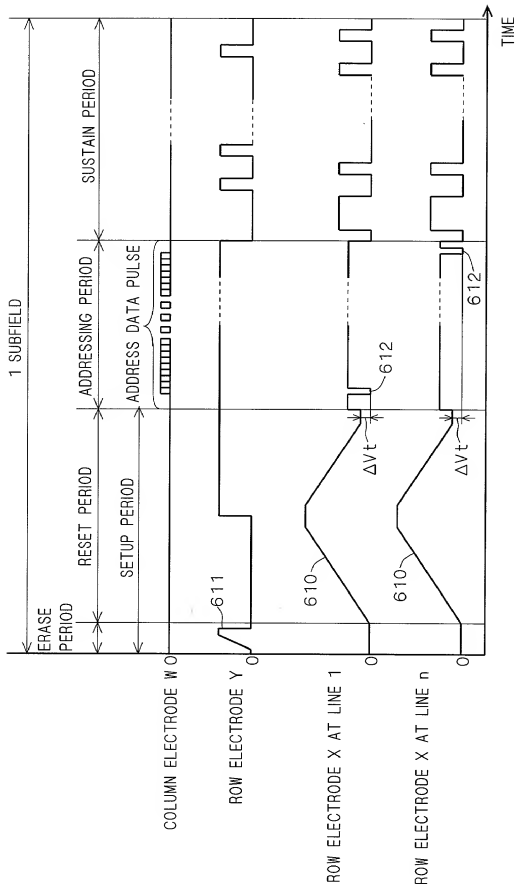
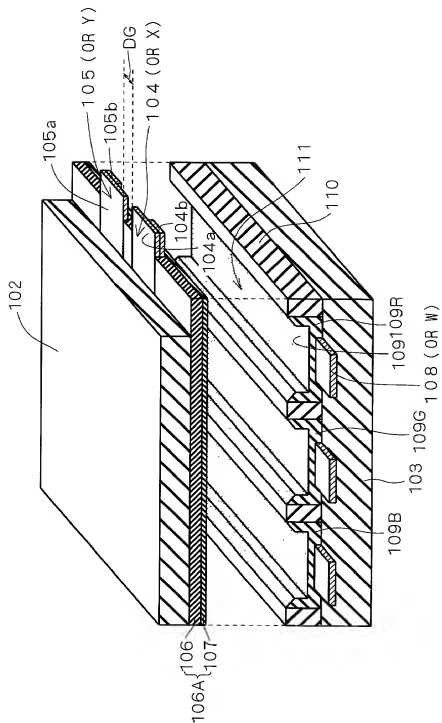


FIG. 28

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The diagram illustrates the timing of signals for a memory array. The vertical axis represents TIME, and the horizontal axis represents the sequence of operations. The signals shown are:

- COLUMN ELECTRODE W**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.
- ROW ELECTRODE Y**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.
- ROW ELECTRODE X AT LINE 0**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.
- ROW ELECTRODE X AT LINE 1**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.
- ROW ELECTRODE X AT LINE 2**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.
- ROW ELECTRODE X AT LINE n**: A signal that is active (high) during the Reset Period and Addressing Period, and inactive (low) during the Sustain Period.

The timing diagram is divided into three main phases:

- RESET PERIOD**: The initial phase where the signals are active.
- ADDRESSING PERIOD**: The phase where the signals are active, and the data is being addressed.
- SUSTAIN PERIOD**: The phase where the signals are inactive, and the data is being sustained.

The diagram also shows the relationship between the signals and the time intervals:

- The **RESET PERIOD** and **ADDRESSING PERIOD** are shown as subfields.
- The **SUSTAIN PERIOD** is shown as a subfield.
- The **RESET PERIOD** and **ADDRESSING PERIOD** are shown as subfields.
- The **SUSTAIN PERIOD** is shown as a subfield.

FIG. 30

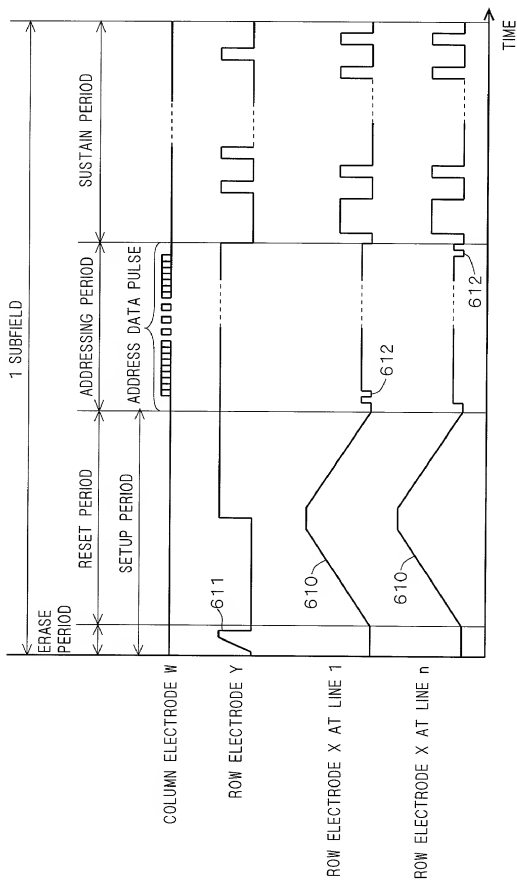


FIG. 31

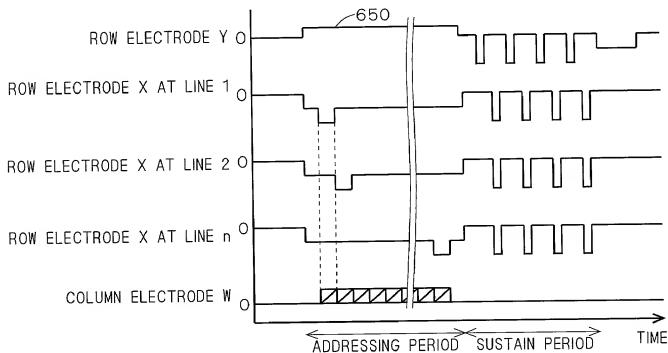


FIG. 32

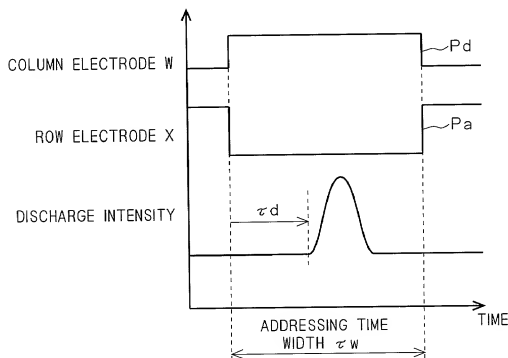


FIG. 33

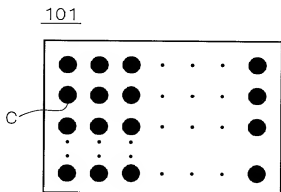


FIG. 34

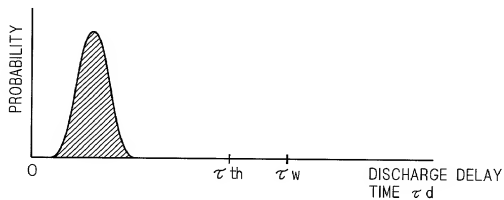


FIG. 35

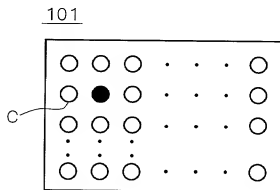


FIG. 36

